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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,501	03/31/2004	Alan R. Ball	ONS00555	4897

7590 10/27/2005

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,501	BALL ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/26/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 09/26/05. A new ground of rejection is introduced as necessitated by amendment.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Asada et al. (USP 5936440).

As to claim 1, Asada et al.'s figure 5 shows a method of forming a self-gated transistor (10) comprising: coupling a transistor (841) operable to form a sense signal representative of a current through the self-gated transistor and configuring a first circuit (840, 501, 7) of the self-gated transistor to disable the transistor substantially upon a positive current flow through the transistor and to enable the transistor responsively to a negative current flow through the transistor. It is noted that col. 6, lines 21-22, teaches that Vr is negative and nearly ground potential. Thus, when Vs is less than Vr, the current flowing through resistor 801 is negative current, and when Vs is greater than Vr, the current flowing through resistor 801 is positive current.

As to claim 2, figure 5 shows that the step of coupling the transistor operable to form the sense signal representative of the current through the self-gated transistor includes forming the transistor having a main transistor portion (10) and a sense transistor (841) as a sensing portion

including coupling the main transistor portion to the sensing portion wherein the sensing portion is operable to form the sense signal representative of the current through the self-gated transistor.

As to claim 3, figure 5 shows that the step of coupling the main transistor portion to the sensing portion includes coupling a drain of the sense transistor to a drain of the main transistor portion and to the drain of the self-gated transistor and also including coupling a gate of the sense transistor to a gate of the main transistor portion and to the gate of the self-gated transistor.

As to claim 4, figure 5 shows the step of configuring the first circuit of the self-gated transistor to disable the transistor substantially upon the positive current flow through the transistor and to enable the transistor responsively to the negative current flow through the transistor includes coupling a comparator (840, 501, 7) to receive the sense signal wherein the sense signal is positive for the positive current flow and is negative for the negative current flow.

As to claim 5, figure 5 shows that the step of coupling the comparator to receive the sense signal includes coupling a non-inverting input of the comparator to have a negative offset voltage (Vr).

As to claim 6, figure 5 shows that the step of coupling the comparator to receive the sense signal includes coupling the comparator to responsively enable the self-gated transistor when the sense signal forms a voltage that is less than a voltage of a source of the self-gated transistor.

As to claim 7, figure 5 shows that the step of coupling the comparator to receive the sense signal includes coupling one of a diode or a resistor (801) between a source of a sense transistor and a source of the self-gated transistor.

As to claim 8, figure 5 shows a method of operating a self-gated transistor comprising: providing an MOS transistor having a main transistor portion (10) and a sensing portion (841)

including coupling the main transistor portion to the sensing portion wherein the sensing portion is operable to form a first sense signal representative of a first current through the main transistor portion; configuring the self-gate transistor to detect the first sense signal and responsively disable the self-gated transistor; configuring the self-gate transistor to conduct a second current through the sensing portion as a second sense signal wherein the second current flows in a direction opposite to the first current; and configuring the self-gate transistor to detect the second sense signal and responsively enable the self-gated transistor.

As to claim 9, figure 5 shows that the step of configuring-the self-gate transistor to conduct the second current through the sensing portion as the second sense signal includes ' configuring the self-gate transistor to steer the second current to flow through a diode (diode that connected to transistor in 841).

As to claim 10, figure 5 shows that the step of configuring the self-gate transistor to conduct the second current through the sensing portion as the second sense signal includes configuring the self-gate transistor to steer-the second sense current to f low through a resistor (801).

As to claim 11, figure 5 shows that the step of configuring the self-gate- transistor to detect the first sense signal and responsively disable the self-gated transistor includes ' ' coupling an input of a comparator (840, 501, 7) to receive the first sense signal.

As to claim 12, figure 5 shows a self-gated transistor comprising: a transistor having a main transistor portion (10) and a sensing portion (841) wherein the sensing portion is coupled to the main transistor portion to form a sense signal representative of a current through the self-gated transistor, the main transistor portion having a first gate; and a control circuit (840, 501, 7)

coupled to receive the sense signal and drive the first gate to enable the transistor responsively to a first polarity of the sense signal and to disable the transistor responsively to an opposite polarity of the sense signal.

As to claim 13, figure 5 shows that the control circuit includes a comparator having an inverting input coupled to receive the sense signal.

As to claim 14, figure 5 shows that the comparator has a non-inverting input coupled to a source of the self-gated transistor.

As to claim 15, figure 5 shows that the non-inverting input of the comparator has a negative offset voltage (Vr).

As to claim 16, figure 5 shows that the sensing portion is a portion of the main transistor portion with a source of the sensing portion separated from a source of the main transistor portion and wherein the main transistor portion and the sensing portion have a common drain.

As to claim 17, figure 5 shows that the sensing portion having a source that is separate from a source of the main transistor portion and a protection circuit (840, 501, 7) coupled to the source of the sensing portion.

As to claim 18, figure 5 shows that a source of the main transistor portion is coupled to a source of the self-gated transistor.

As to claim 19, it is inherent for figure 5 to have a voltage regulator (circuit, not shown) coupled to provide an operating voltage to the comparator and coupled to a source of the self-gated transistor (the comparator must be powered in order to operate, the circuit, not shown, that powers the comparator is considered as the voltage regulator).

As to claim 20, figure 5 shows that the self-gated transistor formed in a package having no greater than four leads.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
Art Unit 2816

October 25, 2005